Vanadium-dioxide thin film based nanoelectronics

(Final report of project Nº NN-110867 by Dr. Mizsei János)

Conventional analog and digital electronics are based only on electric signal processing. However, the thermal state of an electron device may represent information too. At the nanometer scale, heat propagation can be extremely fast, which makes thermal computing an emerging field of research.

We proposed and patented a new active device (phonon transistor = phonsistor) and a phonsistor based thermal electric logic circuit (TELC). These devices are made up of only bulk type intrinsic domains, consisting of significantly fewer regions and interfaces compared to standard complementer MOS (CMOS) based systems.

The basis of TELC operation is the thermal or hot electron coupling between electron devices containing metal-insulator transition (MIT) or semiconductor-metal transition (SMT) material, i.e. VO_2. The physical appearance and the operation of TELC are somewhat analogous with the neuron.

Integration the TELC with CMOS (more than Moore principle) may extend computing ability of the system, as both the thermal and electrical signals are available for information processing.

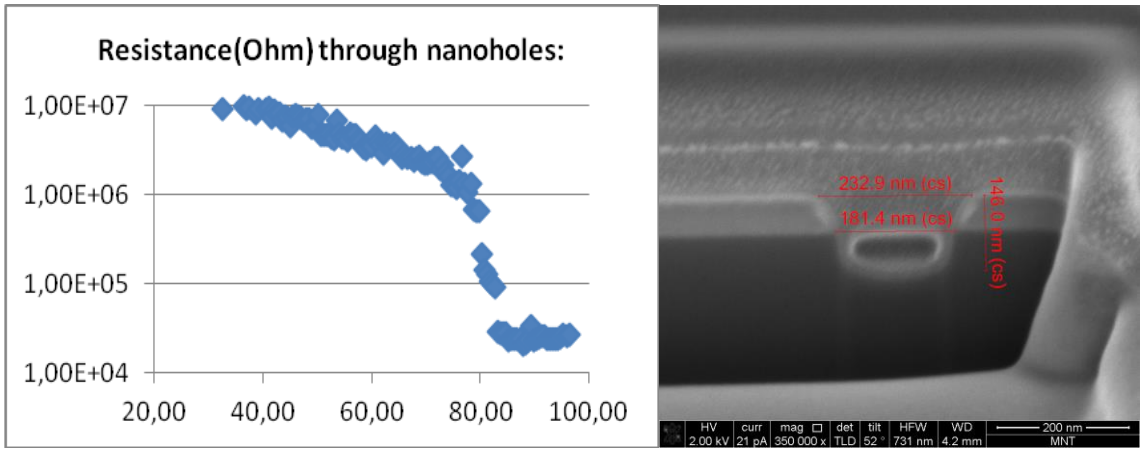
This final report details some efforts on developing the SMT capable VO_2 layer technology, characterisation, TELC device realisation and computer modelling, according to work packages defined in the research plan (see texts in *italic*).

Work Package 1 (WP1): Layer preparation and characterization.

In this work package we aim to compare different VO_2 thin films in terms of applicability as thermally and electrically operated switching devices. Based on extensive literature study different sample preparation methods will be tested, such as reactive ion sputtering, solgel spinon with annealing and pulsed laser deposition (PLD). Some deposition (like the PLD process) and some characterization steps will be performed at the facilities of our cooperating partner, the University of Oulu (Finland). In addition to normal meetings we intend to enhance the cooperation with annual research visits of 1-2 months in Oulu. In other cases the samples will be prepared in the new clean room of our Semiconductor Technology Laboratory (FTL, Félvezetőtechnológiai Laboratórium) using our existing equipment. The characterization analyses include structural, electrical and optical investigations, like mapping different properties of the thin film surface, IV characteristics as function of temperature, and optical transmittance and reflectance and the changes of them following phase transition.

Microelectronics Lab. of the Univ. of Oulu deposited the metal-insulator transition capable VO_2 layers by laser ablation, and structured them by laser and focused ion beam processes. At the preliminary stage of investigation their technology and samples were used to investigate the SMT effect.

SMT phenomenon through nanoholes has successfully been demonstrated (Fig. 1. a.) on laser ablated VO_2 layers deposited into Ga ion beam drilled nanoholes (Fig. 1. b.) in SiO_2 dielectric layer over monocrystalline silicon.

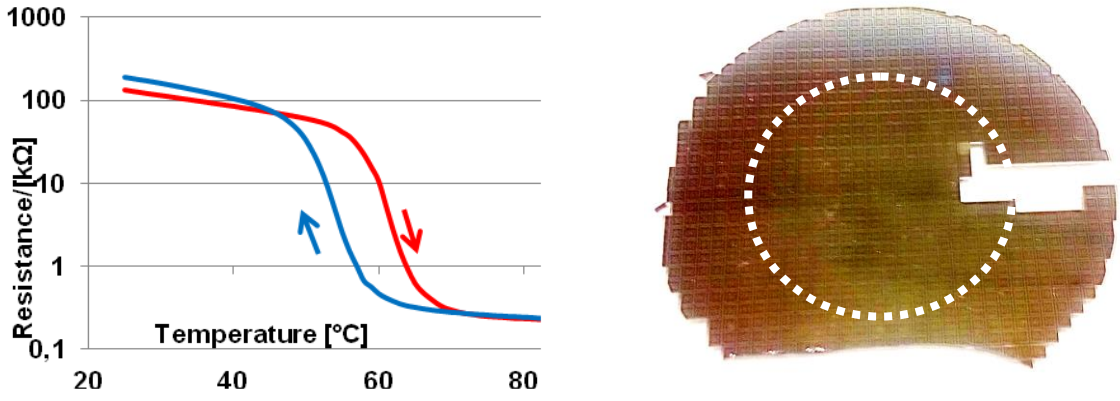


(a) (b)

Figure 1. SMT: Resistance – Temperature plot (a) of a vertical VO_2 resistor deposited into nanohole (b) by laser ablation

To increase our device construction possibility we developed our own deposition technology for SMT capable VO_2 layer. Reactive radio frequency (RF) sputtering has been used for VO_2 synthesis from metallic vanadium target in Ar-O_2 gas mixture. Preliminary experiments were not successful, there was vanadium-oxide layer over the substrate, but no SMT was detected. X-ray diffraction and Raman spectroscopy proved some vanadium-oxide phases, but the layer quality was not suitable for SMT devices. We isolated the substrate from the cooled substrate holder to keep it higher temperature, but these experiments were not successful either.

The problem is solved by mounting a regulated temperature hotplate into our sputtering system. Keeping the substrate surface at 650 °C, we are able to deposit proper SMT capable thin (50-80 nm) films (see. Fig.2.). Our RF sputtering technology resulted in uniform layers over somewhat higher area (~5 cm^2, see dotted white circle in Fig. 2. b. over the photo of a VO_2 layer on a 5 cm diameter wafer) compared to laser ablated ones (1 cm^2) produced by our partner in Oulu, but the SMT effect was not so strong in the case of our layers. However the semiconductor state resistance and metal state resistance ratio is higher than two orders of magnitude, thus the layer seems to be suitable for producing thermal-electronic devices.



(a) (b)

Figure 2. Resistance – Temperature plot of RF sputtered VO_2 layer (a), photograph demonstrating of homogeneity of VO_2 layer (b)

For the sol-gel process we prepared two different precursor solution (V_2O_5, oxalic acid, deionised water and V_2O_5, hydrogen-peroxide). After ageing the solution, thin layers were fabricated by spin-on deposition. Next steps were drying (300°C) and annealing (750°C) in different atmospheres. As these experiments were not successful (no SMT effect was found), we did not produce any phonsistor-like device from these layers.

We did a lot of experiments to discover our VO_2 layer properties for the future device application. Al and Pt metal layers have been used for electrical contacts, only the Pt was suitable material, because of high local thermal stress destroyed the Al contacts.

The SMT could be observed by optical methods too, as the VO_2 layer transmittance and reflectance change drastically during this process. Using optical microscope a thin, dark conducting channel (metallic) could be observed at the beginning of the switching process, while at higher power level the whole surface changed its character to metallic (dark).

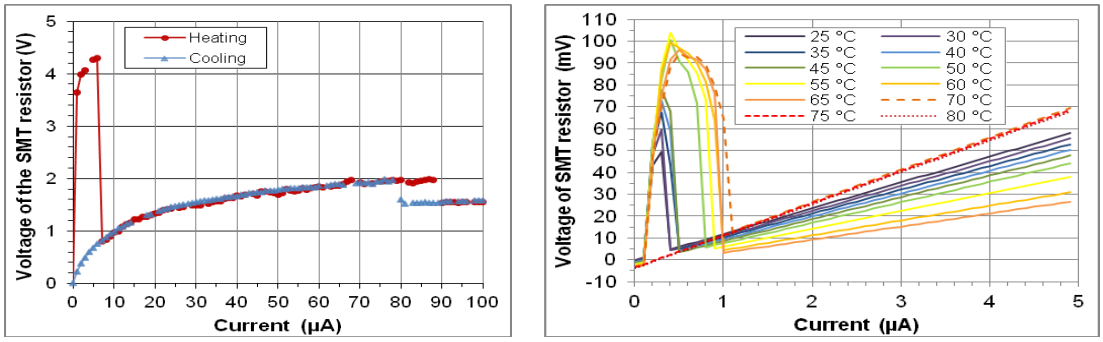
Structuring of VO_2 layers is also very important to build a complex thermal-electronic system. For this purpose, a photoresist/etching technology have been developed: the VO_2 layers can be etched away by H_2O_2 solution through photoresist mask which is resistant against the etching agent.

Work Package 2 (WP2): Device preparation and characterization.

This work package can be summed up as formation and characterization of discrete switching devices based 4 on the SMT (semiconductor – metal transition) behavior of VO_2. The most appropriate film processed in WP1 will be selected, however, simple layer analysis will not show certainly the ability for patterning. Our aim is to form operational devices with characteristic lateral dimension in micrometer scale which is expected to be carried out using our facility. The characterization of the devices will be dominantly electrical. As our targeted lateral feature size of contact electrodes is about few microns it is necessary to use a precise probe station. Electrical measurements will be analyzed as a function of temperature as well; the attached offer shows a probe station which could be upgraded later with a hot chuck system. Using the probe station more samples could be measured effectively, because dicing, die and wire bonding of the samples won't be necessary for characterization, thus it would save human and infrastructural resources.

As we had not got proper VO_2 layer technology at the beginning, we started the work with the above mentioned samples produced by Microelectronics Lab. of the Univ. of Oulu. Figure 3. demonstrates the switching effects of submicron size (see Figure 1.) laser ablated VO_2 thermal electronic devices, i.e. vertical Pt-VO_2-n^{++}Si layer structure.

Irreversible switching behaviour could be observed in the case of forward bias, this experiment destroyed the device, probably due to high applied power density. In the case of reverse bias the thyristor like switching behaviour appeared at extremely low voltage/current/power levels. The switching voltage increases with increasing temperature, thus the switching process is not related to the Joule heating. The theoretical background of that kind of switching behaviour has not been cleared. As the holes in the SiO_2 were drilled by Ga ion beam, that structure may contain a series pn^{++} junction which can inject hot electrons by tunnelling. This device could be an extremely important new electronic component, if it is possible to fabricate it with good reproducibility, because of low switching voltages.



(a) (b)

Figure 3. Irreversible switching behavior (a) of the nm-sized, vertical SMT resistor structure at room temperature and forward bias (positive with respect to n^{++} Si substrate) , and reversible switching behavior (b) of the nm-sized, vertical SMT resistor structure at different temperatures and reverse bias (negative with respect to the n^{++} Si substrate). It can clearly be seen that for 75 °C and above no high-resistance region is present

Laser ablated lateral VO_2 resistors have been produced by Ga ion beam etching and laser beam cut of Pt metal electrodes (see Figure 4.). The VO_2 resistor and a series resistor was powered by a linear voltage ramp (orange line), the voltage of the VO_2 resistor is registrated (blue line). The switching process can clearly be seen from the sudden drop of the VO_2 resistor voltage. The switching time constant is less, than 1 microsecond. This result supports the scaling down assumption, i. e. the thermal time constant scales down proportionally with linear dimensions:

heat capacitance (~l^3) x thermal resistance (~$1/l^2$) = thermal time constant (~l)

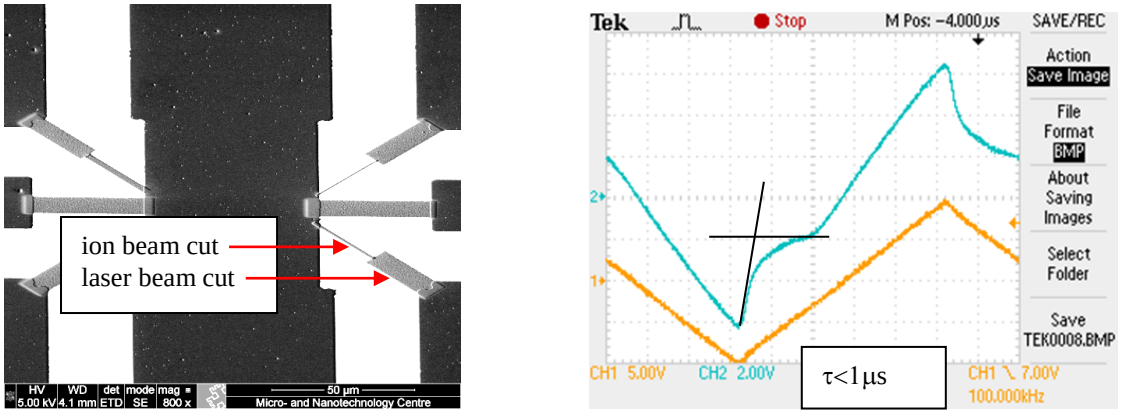
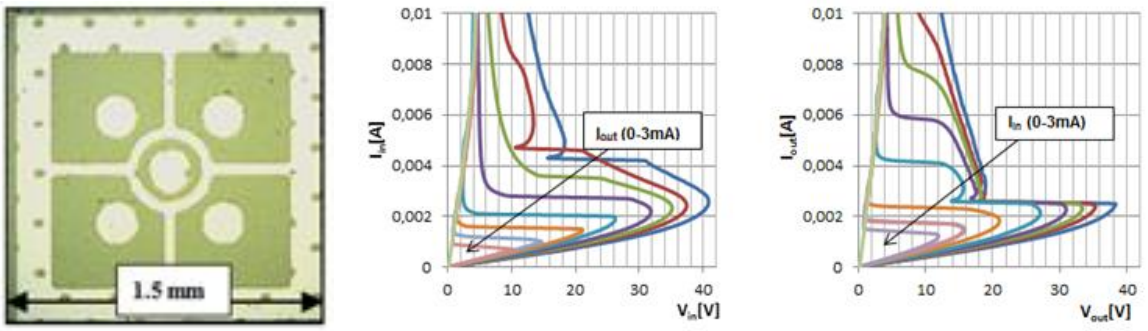


Figure 4. Switching behavior of the submicron-sized, lateral SMT resistor structure at room temperature. The scanning electron micrograph of the structure (a), the power supply voltage (orange) and the voltage on the VO_2 resistor (blue) registered by an oscilloscope (b).

Many different metallisation layout have been designed and tested to realise a VO_2 phonsistor gate, the best one is shown in the Figure 5 (a). The outer (Pt) frame connected to the inner ring is the ground, the dot at the middle is the output, four dots around are inputs. This configuration completely separates the inputs and output electrically, they are only coupled thermally to each other. Input and output I-V characteristics of this phonsistor chip is plotted in Figure 5 (b) and (c) respectively.

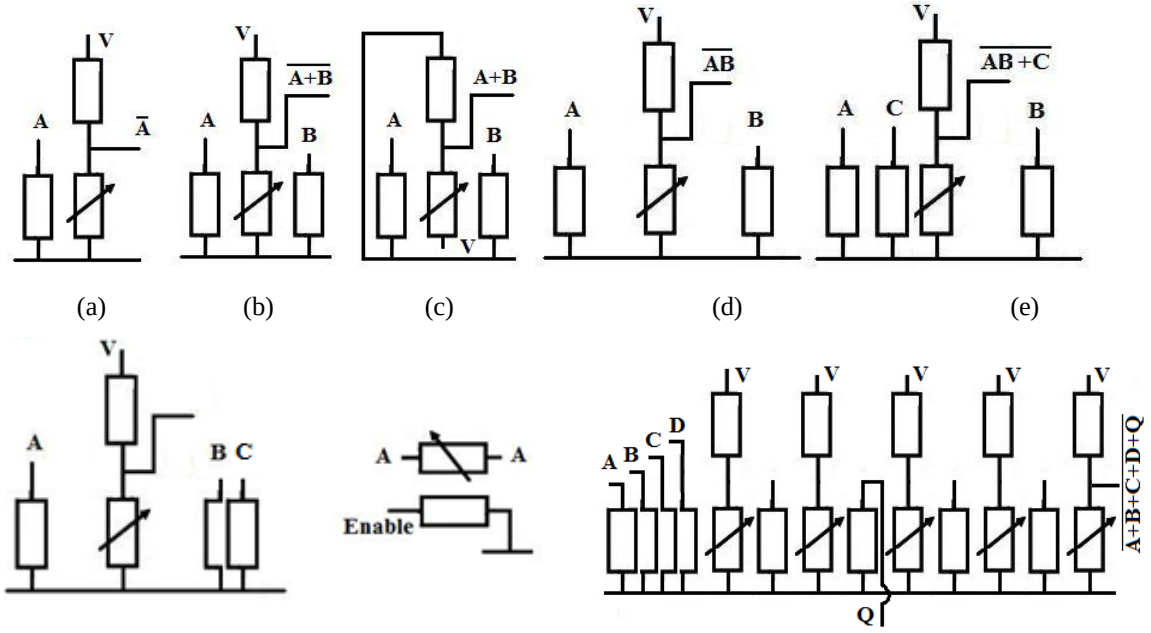


(a) (b) (c)

Figure 5. The cathode sputtered VO2 based phonsistor chip (a), the input (b) and the output (c) I-V characteristics at 35 centigrade, parameters are the output and input currents, respectively

The output of the above shown TELC chip can be switched on by every input independently, thus it realises basically a NOR logic function. However, the TELC conception is more flexible, as the thermal information transfer enables a wide variation of gate realisation. It is not necessary to establish a galvanic connection between components, moreover all terminals of components can be grounded, floating or connected to the power supply (see Figure 6. for practical examples). Also the input resistor can be realized as an MIT device; in that case the input of the gate may keep the information too.

Calculating the total number of components in a TELC system, one can conclude that it is the sum of total number of logic inputs and the number of TELC gates: every TELC gate contains at least one VO_2 resistor switch at the output, and as many heating resistors as number of logic inputs.



(a) (b) (c) (d) (e)

(f) (g) (h)

Figure 6. Thermal electric logic circuits (TELCs): inverter (a), NOR (b), OR (c), NAND (d), inverted AND-OR (e), majority (f), transfer gate (g), thermal transmission line with a four input NOR gate at the beginning of the inverter chain

As a good TELC test and modell system, the thermal transmission line (like Fig.6.(h)) is realised using nine TELC chips mounted nearby each other (Fig. 7). The accelerated heat transfer and the thermal signal recovery through signal propagation have been demonstrated

on that thermal – electronic circuit. All output was powered by voltage source through a pull up resistor, than the first gate switched on. The total current through the system shows the switching process propagation (see Fig. 8).

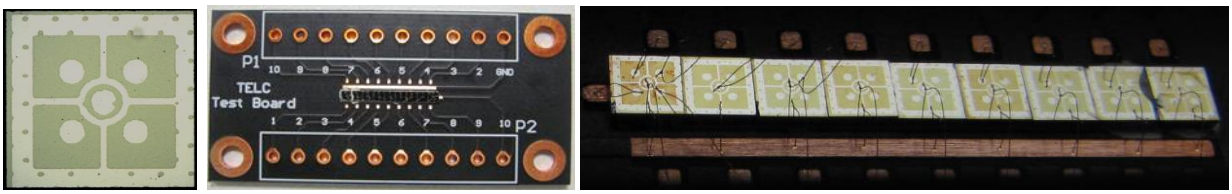


Figure 7. The photograph of the TELC gate chip (a), the PCB test board (b) and the TELC based thermal transmission line (c) (nine gates thermally coupled, mounted on the test board)

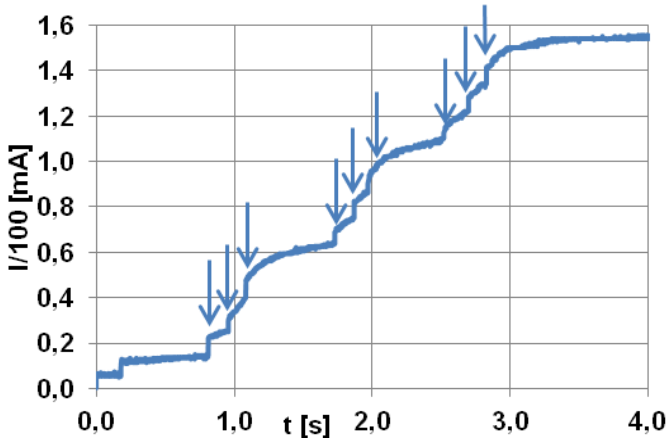


Figure 8. The total current of the nine, thermally coupled TELC chips switching on one after another. The first step is related to the "power on", the next nine arrow marked steps show the propagation of the switching on process

The thermal signal propagation speed can be increased by applying higher power supply voltage. Table I. summarizes the delay times after the first gate activation. At lower power supply voltage the last gate does not switch at all. Higher supply voltage results in a virtual heat conductance increase.

Power supply voltage	Gate2	Gate4	Gate9
5	0,16	1,95	no switch
10	0,10	1,48	10,14
15	0,12	1,08	4,31
25	0,07	0,54	1,57

Table I. Thermal signal propagation speed among the thermal transmission line: delay times in seconds after the first gate activation

The basic operation mode of the TELC is digital. However, analogue operation of the phonsistor is also possible. There are negative differential resistance regions in the output I-V plot (see Fig. 5. c), thus it is proper component for oscillator circuits.

Completing this work package, we purchased and installed a probe station with proper pin contact system and thermostat for measuring our chips before encapsulation. A SEM

system with electron beam mask generation also installed for producing submicron thermal electronic circuits.

Work Package 3 (WP3): Electro-thermal modeling and simulation.

Electro-thermal modeling and simulation of layered SMT structures and devices may reveal the behavior of active layers, multilayer structures considering the role of substrate and contact layers and complex device structures containing multiple SMT devices and heating elements. Based on the results of the simulation one can report about the possibility of constructing IC with SMT devices. For simulation purposes we plan to use ANSYS Multiphysics and SUNRED, a very fast electro-thermal simulation software developed and continuously improved by our department.

Simulation is very important part of the complex system design: the operation of thermal-electric circuits largely depends on the arrangement, size and spacing of the circuit elements, simulation is required to test the proper behaviour of the device. Criterion of the simulation is a model that can accurately describe the operation of an SMT device.

The big challenge of TELC simulation is, that the resistivity of VO_2 changes 30-40% by 0.1 K temperature change in the transition region. If a real-world device model is simulated, conventional simulators (ANSYS, COMSOL) tends to diverge, we also experienced this. To avoid divergence there are two ways: restrict the model or change the simulation method. In the referenced papers restrictions could be applied because of the investigated problems but in case of TELC simulations this is not an option. Thermal-electronic circuits must work on the top of normal silicon chips, and their behaviour should be investigated in such environment.

To be able to handle divergence problems, we have extended the SUNRED, a very fast electro-thermal simulation software developed and continuously improved by our department. This is the first ever publication of an electro-thermal transient simulation method for VO_2 devices operating in real-world conditions.

We have developed three SMT models (hysteresis, *R(T)* function and broken line). The hysteresis model and the *R(T)* function can be used in later works, broken line model seems less useful.

A 200 µm × 20 µm area sized VO_2 resistor with about 50 nm thickness, deposited on a silicon substrate was characterised, modelled and simulated by the SUNRED simulator. Figure 9. shows the voltage-current measurement and simulation results of the VO_2 resistor. The results show an acceptable agreement with the measurement results, the difference is due to the finite resolution of the model. In the simulation a one cell wide channel formed.

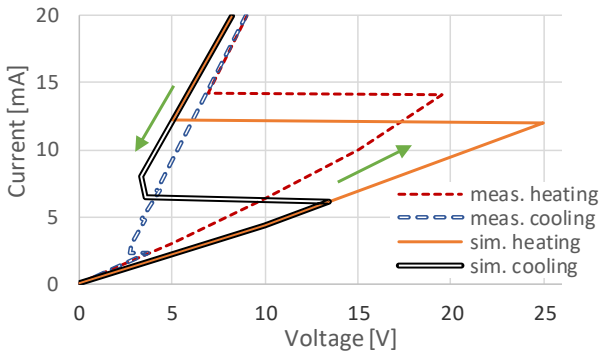


Figure 9. Measured and simulated voltage-current curves (hysteresis R-T model)

Our complex, physically realised thermal-electrical circuit structure (see photo in Fig. 7.) was modelled by SUNRED. The simulated switching characteristics can be seen in Fig. 11. calculated for the four input resistors and the output resistor, respectively.

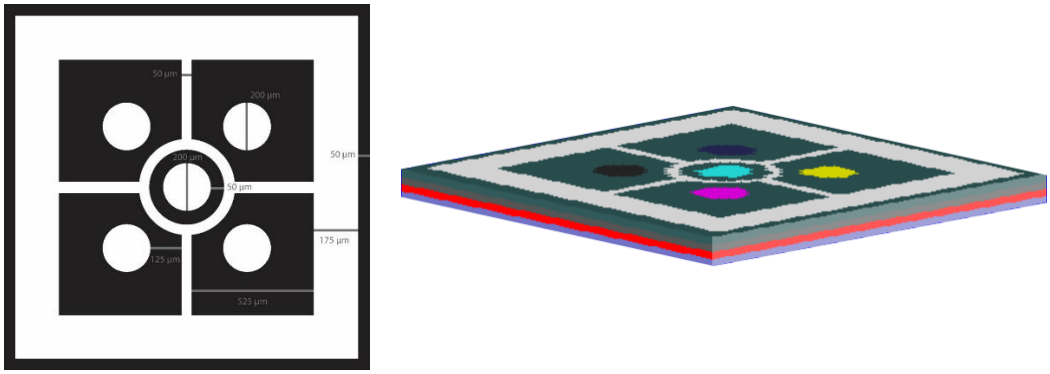


Figure 10. A complex TELC structure and the SUNRED model.

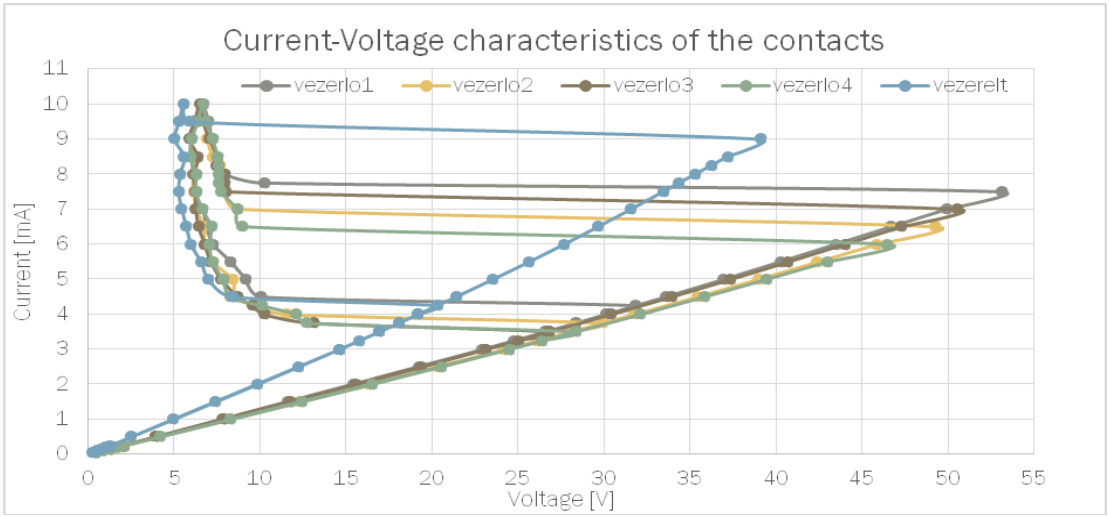
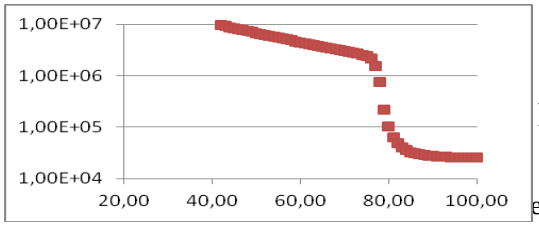


Figure 11. Simulated characteristics of the complex TELC structure

The goal of the research work has been achieved, i.e. we have created sufficiently accurate SMT models and a simulator capable of investigating SMT devices and thermal-electrical structures. As a next step in simulation and modelling we want to carry out further research in two directions. As a result of the strong nonlinearities, the simulation times are very long: generation of I-V characteristics can take 10-20 hours or more, depending on the resolution and detail of the models. Our purpose is to speed up the simulations significantly by applying new algorithms. SMT models are sensitive to resolution: the lower resolution than necessary decrease accuracy significantly. If the resolution is too high, the simulation times can increase unacceptably. So we would like to find the optimal resolution of the models.

Most of thermal modelling software works with linear broken line approximation of Resistance – Temperature function. We found a semi-empirical mathematical formula for modelling of the SMT process (see equation and R-T plot in Fig. 12).



$$R = \left(-a \frac{T-b}{\sqrt{(T-b)^2}} \frac{(T-b)^c}{(T-b)^c + d} + a \right) \exp \frac{e}{T} + g$$

ed by equation above (a=3, b=350.5 K, c=2, d=0.5, e=4500 K which corresponds to ~0.8 eV activation energy in semiconductor state, g=25 kΩ which is the resistance in the metallic state

This model correctly describes the R-T plot in the semiconductor state by activation energy (e), the SMT temperature by (b), the resistance in the metallic state by (g). Other parameters are related to the slope of the curve during the SMT process, and the resistance drop.

Summary

Comparing the work packages and results, one can conclude, that most of the project targets has been investigated in details. The project support was very important to improve our technological and measurement facilities to promote the future work on that field.

More than ten students from different countries were involved into this research work in the frame of project laboratory, BSc and MSc thesis preparation.

The most important achievements and results, as well as unsuccessful attempts are summarised below.

“Success” list:

WP1: SMT capable VO_2 deposition technology by reactive sputtering and photoresist/etching technology for VO_2 layers have been developed; SMT phenomenon through nanoholes has been demonstrated

WP2: switching effect of nanometer and micrometer size thermal electronic device and logic operation the TELC devices has been demonstrated, input and output I-V characteristics of a phonsistor chip has been plotted, basic set of TELC gates has been worked out, the accelerated heat transfer and the thermal signal recovery through the thermal transmission line was demonstrated

WP3: an empirical mathematical formula was worked out for SMT process; different layered TELC structures have been modelled

“Failure” list:

WP1:
Sol-gel preparation of SMT VO_2 layers

WP2:
Switching mechanism of the nano sized device has not been completely understood

WP3: -